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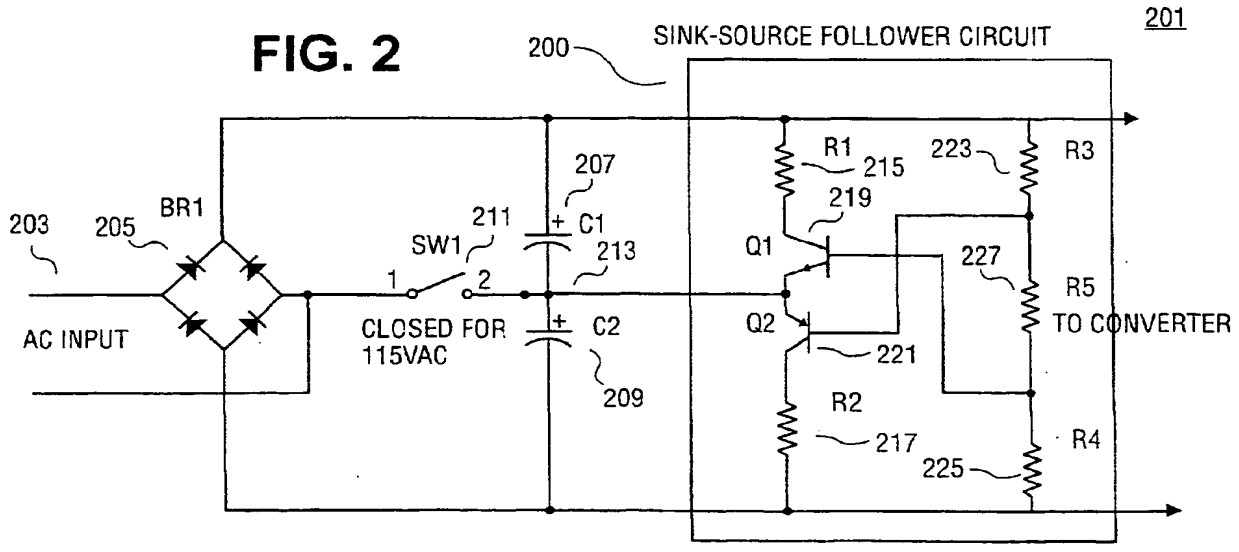
(54) Method and apparatus for balancing active capacitor leakage current

(57) A circuit 201 that provides a method and apparatus to actively balance capacitor leakage current from series stacked capacitors 207, 209 and disconnects itself when stacked capacitors are configured for doubler operation. In one embodiment, the active circuit includes high voltage low current transistors, such as for example a PNP bipolar transistor 221 and an NPN bipolar transistor 219, that are configured in a sink-source voltage follower arrangement 200 with the bases of the transistors 219, 221 connected to a voltage divider network and referenced to a fraction of a DC input voltage with a very high impedance, low dissipative resistor divider network. In one embodiment, the emitters of the PNP and NPN transistors are both tied to the connection point 213 between capacitors 207, 209 in the stack and provide an active sink-source drive, which maintains the voltage at this point to be bounded by the input reference voltages of sink-source followers.

FIG. 2



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Description

[0001] This invention relates generally to circuits and, more specifically, the present invention relates to circuits including series stacked capacitors.

[0002] One function of a power converter is to convert rectified alternating current (AC) power into a regulated direct current (DC) output. Figure 1 shows elements included at an input 103 to a power converter 101. Diode bridge BR1 105 rectifies AC input. Series stacked capacitors C1 107 and C2 109 are coupled across diode bridge BR1 105 to smooth the output voltage of diode bridge BR1 105. Series stacked capacitors are common in power supplies that can be configured to operate using multiple different input voltages such as for example either 115VAC or 230VAC. As shown, switch SW1 111 is coupled between diode bridge BR1 105 and the connection point 113 between series stacked capacitors C1 107 and C2 109. When operating for example at 230VAC, switch SW1 111 is opened. When operating for example at 115VAC, switch SW1 111 is closed.

[0003] Resistors R1 115 and R2 117 are coupled across series stacked capacitors C1 107 and C2109 as shown to maintain roughly equal voltages across C1 107 and C2 109 and provide the necessary bleed current needed to balance the voltage across series stacked capacitors C1 107 and C2 109 when the supply is configured for 230VAC input. During 115VAC operation, the two series stacked capacitors C1 107 and C2 109 function as part of an input voltage doubler circuit. When configured for 230VAC, however, the two series stacked capacitors C1 107 and C2 109 have no DC connection to a center point voltage other than that which is provided by resistors R1 115 and R2 117. Without resistors R1 115 and R2 117, the center point voltage of the two series stacked capacitors C1 107 and C2 109 can deviate from the ideal ½ DC input due to capacitor leakage current, which can cause one capacitor to have more voltage stress than the other capacitor. In fact, it is possible that one of the capacitors can be over-voltage stressed and become damaged.

[0004] Resistors R1 115 and R2 117 therefore provide a solution to the balance problem by providing bleed current. The resistance values of R1 115 and R2 117 must be low enough to establish a bleed current that is several times higher than the worst case leakage current imbalance between the series stacked capacitors C1 107 and C2 109 in order to be effective. This requires the resistors to dissipate much more power than the actual power dissipated as a result of the difference current between the two capacitors. Consequently, resistors R1 115 and R2 117 result in significant input power consumption with respect to many standby or output no-load requirements of a power supply converter coupled to receive the rectified AC power.

[0005] It is an object of the invention to seek to mitigate this disadvantage.

[0006] According to a first aspect of the invention there is provided a circuit comprising a first transistor coupled across a first capacitor included in a series of stacked capacitors and a second transistor coupled across a second capacitor included in the series stacked capacitors, the first transistor coupled to the second transistor, the first capacitor coupled to the second capacitor, wherein the first and second transistors are adapted to provide a bleed current to the series of stacked capacitors to balance a leakage current imbalance in the series of stacked capacitors.

[0007] According to a second aspect of the invention there is provided a method comprising providing a bleed current through a first transistor to a connection point between first and second capacitors included in a series of stacked capacitors if a voltage at the connection point rises above an upper reference voltage, and providing the bleed current through a second transistor to the connection point if the voltage at the connection point falls below a lower reference voltage.

[0008] According to a third aspect of the invention there is provided a circuit comprising a series of stacked capacitors including first and second capacitors coupled across a power supply input, a first transistor coupled across the first capacitor, the first transistor having a control terminal coupled to receive a first reference voltage, and a second transistor coupled across the second capacitor, the second transistor having a control terminal coupled to receive a second reference voltage, the first and second capacitors coupled to the series of stacked capacitors at a connection point between the first and second capacitors, the first and second transistors adapted to provide a bleed current to balance a leakage current imbalance in the series of stacked capacitors.

[0009] Thus, using the invention it is possible to provide an active circuit that substantially reduces the bleed current required for balancing leakage current in series stacked capacitors. This active circuit can also be designed to disconnect any bleed current when capacitors are configured for voltage doubler operation as bleed current is not necessary in this configuration. In one embodiment, the circuit may be switched across a capacitor to provide bleed current as required to balance the leakage current. In one embodiment, the voltage at the connection point between two capacitors may be bounded within a few volts of two reference voltages. In one embodiment, the bleed current may be substantially equal to the difference in leakage current between two series stacked capacitors. In one embodiment, the active circuit suitably includes a sink-source follower circuit. In one embodiment, a sink-source follower circuit can include inputs where each are referenced to voltages that are offset by a fraction of the voltage applied across the series stacked capacitors and the outputs of the sink-source follower circuits are coupled to the connection point between two series stacked capacitors. In one embodiment the offset is preferably limited to a very low value and can be substantially zero. In one embod-

iment, the sink follower circuit may include a PNP bipolar transistor coupled to a source follower circuit, which includes an NPN bipolar transistor. In one embodiment, resistors are suitably connected in series with the collector of each of the bipolar transistors to limit the peak current conducted by the bipolar transistors. In one embodiment, the active circuit is suitably used in a power supply circuit.

[0010] In another embodiment, a method of substantially reducing the bleed current required for balancing leakage current in series stacked capacitors utilizing an active circuit is disclosed. In one embodiment, the bleed current may be switched in as required to balance leakage current from the series stacked capacitors. In one embodiment, the bleed current from the active circuit may be switched off and may be substantially equal to zero when series stacked capacitors are configured for doubler operation. In one embodiment, the bleed current can be substantially equal to a difference in leakage currents between two capacitors. In one embodiment, the active circuit suitably includes a means to maintain an output voltage, connected to the connection point between two series stacked capacitors, relative to an input reference voltage. In one embodiment, the disclosed method is suitably applied in a power supply circuit.

[0011] An embodiment of the invention is hereinafter described, by way of example with reference to the accompanying drawings.

[0012] The present invention detailed is illustrated by way of example and not limitation in the accompanying figures.

Figure 1 shows a circuit schematic of a known technique to balance capacitor leakage current from series stacked capacitors; and

Figure 2 shows one embodiment of a circuit schematic in which capacitor leakage current from series stacked capacitors is balanced in accordance with the teachings of the present invention.

[0013] An embodiment of a circuit schematic that balances active capacitor leakage current is disclosed. In the following description, numerous specific details are set forth in order to provide a thorough understanding of the present invention. It will be apparent, however, to one having ordinary skill in the art that the specific detail need not be employed to practice the present invention. In other instances, well-known materials or methods have not been described in detail in order to avoid obscuting the present invention.

[0014] Reference throughout this specification to "one embodiment" or "an embodiment" means that a particular feature, structure or characteristic described in connection with the embodiment is included in at least one embodiment of the present invention. Thus, the appearances of the phrases "in one embodiment" or "in an embodiment" in various places throughout this specification are not necessarily all referring to the same embodiment. Furthermore, the particular features, structures or characteristics may be combined in any suitable manner in one or more embodiments.

[0015] As an overview, input power dissipation associated with the balancing of leakage current of series stacked capacitors is reduced according to an embodiment of the present invention. In one embodiment, a circuit according to the teachings of the present invention actively balances the voltage of series stacked capacitors using high voltage low current transistors, such as for example one PNP and one NPN bipolar transistor. In one embodiment, the transistors are configured in a sink-source voltage follower arrangement with the bases of these transistors tied to slightly different or offset reference voltages centered near ½ DC input voltage with a very high impedance, low dissipative resistor divider network which includes three resistors. The emitters of the two transistors are both tied to the connection point between series stacked capacitors and provide an active sink-source drive, which bounds the voltage at this point to be within input references.

[0016] To illustrate, Figure 2 shows generally one embodiment of a circuit 201 according to the teachings of the present invention to actively balance the voltage of series stacked capacitors. In one embodiment, circuit 201 is a portion of a power converter or power supply that rectifies and smoothes a high voltage AC input. In the illustrated embodiment, circuit 201 is adapted to be compatible with multiple different input voltages for the power supply or converter such as for example but not limited to 230 VAC or 115 VAC. As shown in the depicted embodiment, diode bridge BR1 205 is coupled to rectify AC input 203 voltage and stacked capacitors C1 207 and C2 209 are coupled across diode bridge BR1 205 to smooth the rectified voltage. As shown, switch SW1 211 is coupled between diode bridge BR1 205 and the connection point 213 between series stacked capacitors C1 207 and C2 209. When operating for example at 230VAC, switch SW1211 is opened. When operating for example at 115VAC, switch SW1 211 is closed to provide voltage doubling across the series combination of C1 207 and C2 209.

[0017] As shown inside box 200 of Figure 2, one embodiment of a sink-source voltage follower circuits are illustrated. The illustrated sink-source voltage follower circuits include a resistor R1 215, a bipolar NPN transistor Q1 219, a bipolar PNP transistor Q2 221 and a resistor R2 217 coupled in series across series stacked capacitors C1 207 and C2 209. The control terminals or bases of transistors Q1 219 and Q2 221 are connected through resistor R5 227 and are therefore biased to input reference voltages slightly offset from each other. In one embodiment, the degree of offset of the input reference voltages is provided with a resistor network and is governed by the choice of resistors R3 223, R4 225 and R5 227. When the switch SW1 211 is closed to provide voltage doubling across the series combination of C1

207 and C2 209, the offset introduced by resistor 227 allows transistors Q1 219 and Q2 221 to be effectively disconnected and prevent the circuit from trying to correct for true voltage differences in the voltages applied to capacitors 207 and 209 on subsequent AC half cycles. In one embodiment, resistor R5 may have a resistance substantially equal to zero, which limits the offset to a low or substantially zero value and has the effect of replacing R5 227 with a short circuit connection effectively connecting the bases of bipolar transistors Q1 219 and Q2 221 together. In one embodiment, the resistance values of resistors R3 223, R4 225 and R5 227 are much larger than resistors R1 115 and R2 117 of Figure 1, which reduces the power dissipation in these resistors R3 223, R4 225 and 227 in comparison with resistors R1 115 and R2 117 of Figure 1.

[0018] In the embodiment illustrated in Figure 2, the sink-source follower circuit has its output connected to the connection point 213 between the series stacked arrangement of series stacked capacitors C1 207 and C2 209. Either transistor Q1 219 or Q2 221 will turn on if the voltage at output of the sink-source follower at connection point 213 deviates by more than the upper or lower input reference voltage as defined by the resistor divider network R3 223, R4 225 and R5 227. In this way, the output of the sink-source follower at connection point 213 is maintained within the input reference voltage range defined by R3 223, R4 225 and R5 227. In the embodiment shown in Figure 2, R5 227 offsets the input reference voltages at the control terminals or bases of the transistors Q1 219 and Q2 221 of the sink-source follower such that the base of transistor Q1 219 is slightly below one half the DC input to the series stacked capacitors and the base of transistor Q2 221 is slightly above one half the DC input to the series stacked capacitors. This is to ensure that both transistors will be off when series stacked capacitors are configured for doubler operation with switch SW1 211 closed. In another embodiment, not shown, the reference voltages defined by the choice of resistor R3 223, R4 225 and R5 227 are not centered at one half the DC input voltage to the series stacked capacitors but at some other fraction of the DC input voltage. Resistors R1 215 and R2 217 in Figure 2 are chosen to have much lower resistance than R3 223, R4 225 and R5 227 and limit the power dissipation in the sink-source follower.

[0019] It is appreciated that although the embodiment illustrated in Figure 2 uses a series stack of two capacitors, this circuit could apply to any number of series stacked capacitors where the connection point between each pair of capacitors in the series stack would be connected to the output of a separate sink-source follower circuit in accordance with the teachings of the present invention.

[0020] Therefore, the embodiment illustrated in Figure 2 actively controls the voltages across series slacked capacitors C1 207 and C2 209 where either transistors Q1 219 or Q2 221 maybe on depending on the polarity of capacitor leakage offset. This bleed current provided by the correcting transistor Q1 219 or Q2 221 will be substantially equal to the leakage current imbalance of capacitors C1 207 and C2 209 and therefore the minimum required to perform this function. As a result, dissipation of the balancing circuit is kept to a substantially minimal value.

[0021] In the foregoing detailed description, the method and apparatus of the present invention has been described with reference to specific exemplary embodiments thereof. It will, however, be evident that various modifications and changes may be made thereto without departing from the broader spizit and scope of the present invention. The present specification and figures are accordingly to be regarded as illustrative rather than restrictive.

Claims

1. A circuit, comprising:

   a first transistor coupled across a first capacitor included in a series of stacked capacitors; and a second transistor coupled across a second capacitor included in the series stacked capacitors, the first transistor coupled to the second transistor, the first capacitor coupled to the second capacitor, wherein the first and second transistors are adapted to provide a bleed current to the series of stacked capacitors to balance a leakage current imbalance in the series of stacked capacitors.

2. A circuit according to claim 1, further comprising a resistor divider network coupled to respective control terminals of the first and second transistors to define an input reference for the circuit.

3. A circuit according to claim 2, wherein the resistor divider network comprises at least two resistors coupled to the respective control terminals of the first and second transistors.

4. A circuit according to any preceding claim, wherein the first and second transistors are coupled to a connection point between the first and second capacitors of the series of stacked capacitors, the first and second transistors adapted to maintain a voltage at the connection point within an input reference range.

5. A circuit according to any preceding claim, wherein the bleed current is substantially equal to the leakage current imbalance in the series of stacked capacitors.

6. A circuit according to any of claims 1 to 4, wherein

the bleed current is substantially equal to zero when a voltage at the connection point remains fixed at a voltage within an input reference range.

7. A circuit according to any preceding claim, wherein the first and second transistors are coupled in a sink-source follower circuit configuration.

8. A circuit according to claim 7, wherein the sink-source follower circuit is coupled to receive an input reference that is a fraction of a voltage applied across the series of stacked capacitors.

9. A circuit according to claim 8, wherein the input reference is a range of voltages including upper and lower reference voltages, each of which is offset from the fraction of the voltage applied across the series of stacked capacitors.

10. A circuit according to claim 9, wherein the offset of the upper and lower reference voltages from the fraction of the voltage applied across the series of stacked capacitors is zero.

11. A circuit according to any of claims 7 to 10, wherein the first and second transistors comprise bipolar junction transistors.

12. A circuit according to claim 11, wherein the first and second transistors comprise a PNP transistor and an NPN transistor.

13. A circuit according to claim 12, further comprising a first resistor coupled to a collector of the first transistor to limit the bleed current through the first transistor, the circuit further comprising a second resistor coupled to a collector of the second transistor to limit the bleed current through the second transistor.

14. A circuit according to any preceding claim, wherein the circuit is an active circuit included in a power supply circuit.

15. A method, comprising:

providing a bleed current through a first transistor to a connection point between first and second capacitors included in a series of stacked capacitors if a voltage at the connection point rises above an upper reference voltage; and
providing the bleed current through a second transistor to the connection point if the voltage at the connection point falls below a lower reference voltage.

16. A method according to claim 15, wherein the voltage at the connection point rises above the upper reference voltage as a result of a leakage current imbalance in the series of stacked capacitors, the method further comprising balancing the leakage current imbalance with the bleed current.

17. A method according to claim 16, wherein the bleed current is substantially equal to a difference in leakage currents between the first and second capacitors.

18. A method according to claim 15, wherein the voltage at the connection point falls below the upper reference voltage as a result of a leakage current imbalance in the series of stacked capacitors, the method further comprising balancing the leakage current imbalance with the bleed current.

19. A method according to claim 18, wherein the bleed current is substantially equal to a difference in leakage currents between the first and second capacitors.

20. A method according to claim 15, further comprising maintaining the voltage at the connection point within an input reference voltage range defined by the upper and lower reference voltages.

21. A method according to claim 20, wherein an offset between the upper and lower reference voltages is substantially zero.

22. A method according to any of claims 15 to 21, further comprising smoothing an output voltage of a diode bridge of a power supply with the series of stacked capacitors.

23. A method according to any of claims 15 to 22, further comprising switching off the first and second transistors if the voltage at the connection point is between the upper and lower reference voltages.

24. A circuit, comprising:

a series of stacked capacitors including first and second capacitors coupled across a power supply input;
a first transistor coupled across the first capacitor, the first transistor having a control terminal coupled to receive a first reference voltage; and
a second transistor coupled across the second capacitor, the second transistor having a control terminal coupled to receive a second reference voltage; the first and second capacitors coupled to the series of stacked capacitors at a connection point between the first and second capacitors, the first and second transistors adapted to provide a bleed current to balance a leakage current imbalance in the series of stacked capacitors.

25. A circuit according to claim 24, further comprising:

a first resistor coupled to the first transistor to limit the bleed current through the first transistor, and
a second resistor coupled to the second transistor to limit the bleed current through the second transistor.

26. A circuit according to either of claims 24 or 25, further comprising a resistor network coupled to the first and second transistors to provide the first and second reference voltages.

27. A circuit according to claim 26, wherein the first and second reference voltages provided by the resistor network are different from one another.

28. A circuit according to claim 26, wherein the first and second reference voltages provided by the resistor network are the same.

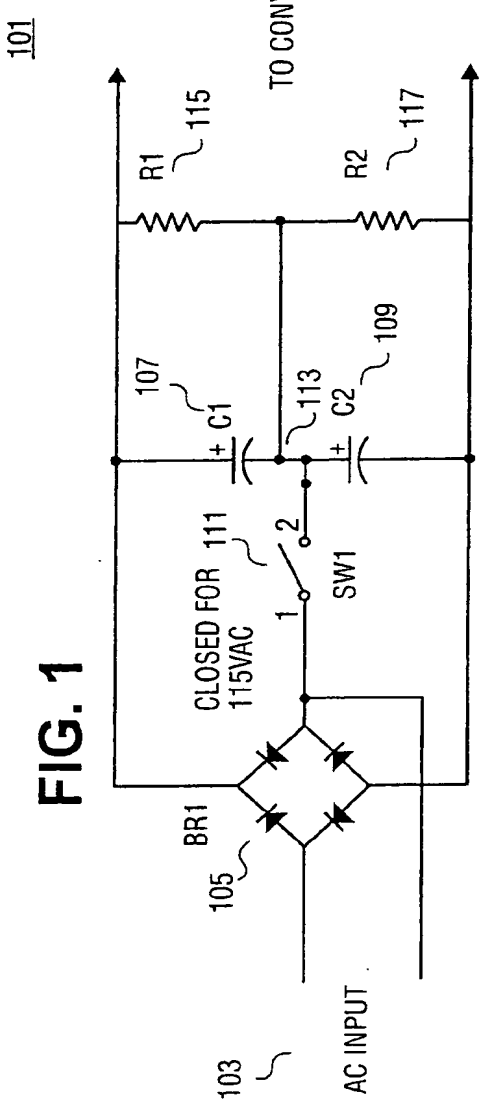

FIG. 1

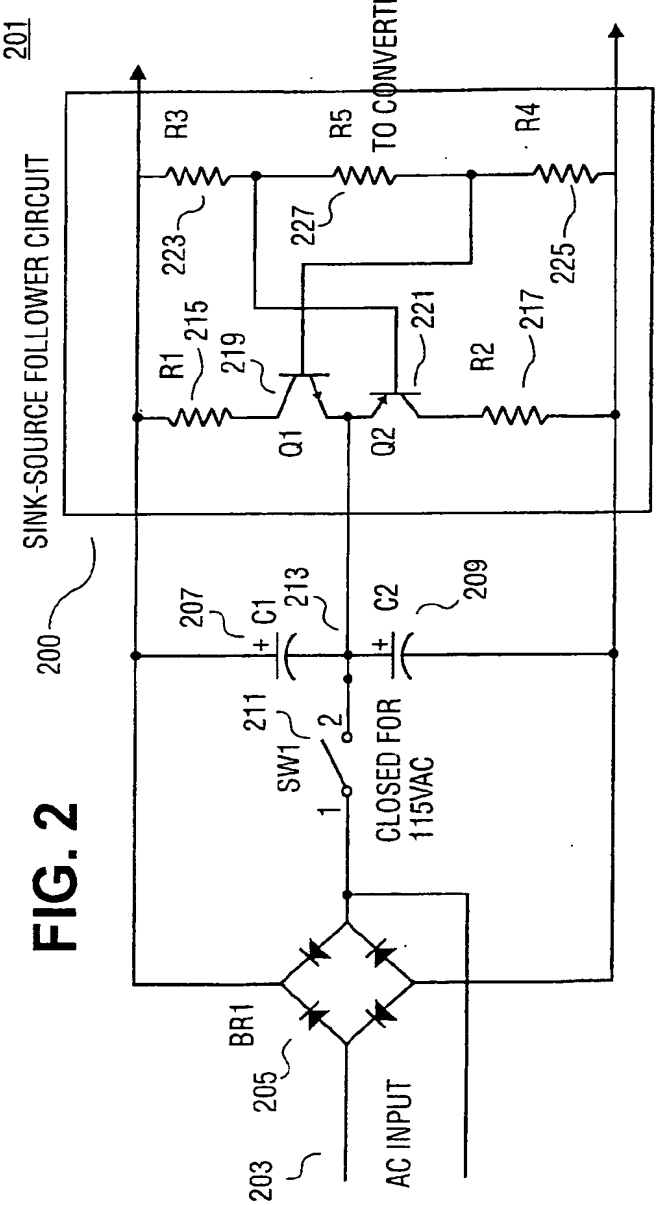

FIG. 2

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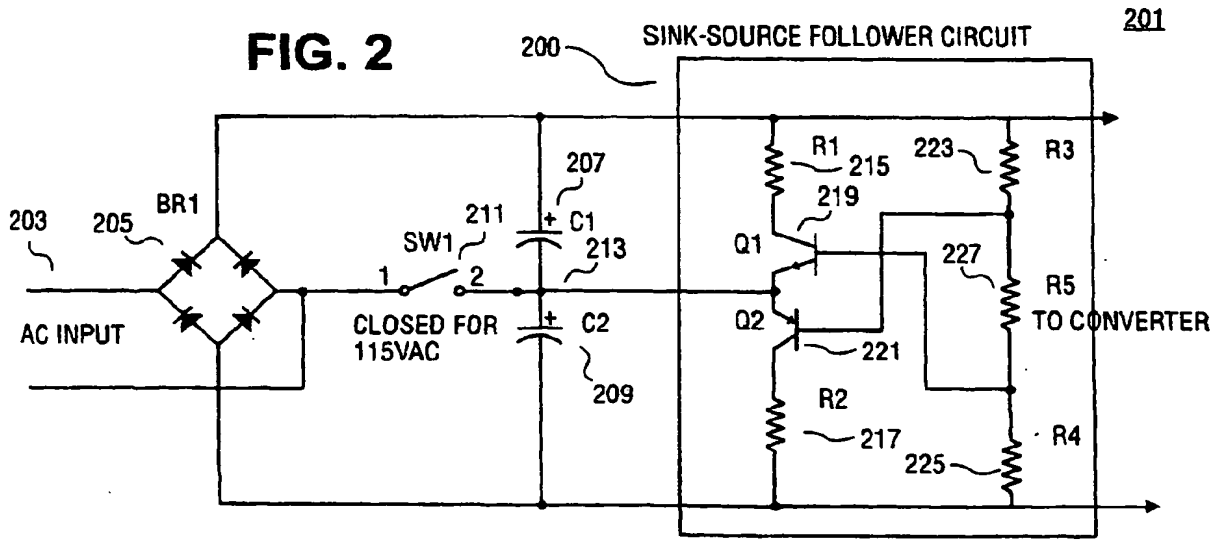
FIG. 2



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EUROPEAN SEARCH REPORT

Application Number
EP 02 25 8114

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Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.7)
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The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
The Hague	26 January 2005	Lund, M

CATEGORY OF CITED DOCUMENTS

X : particularly relevant if taken alone
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A : technological background
O : non-written disclosure
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			TECHNICAL FIELDS SEARCHED (Int.Cl.7)

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
The Hague	26 January 2005	Lund, M

CATEGORY OF CITED DOCUMENTS

X : particularly relevant if taken alone
Y : particularly relevant if combined with another document of the same category
A : technological background
O : non-written disclosure
P : intermediate document

T : theory or principle underlying the invention
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D : document cited in the application
L : document cited for other reasons

& : member of the same patent family, corresponding document

EPO FORM 1503 03.82 (P04C01)

European Patent Office

Application Number
EP 02 25 8114

CLAIMS INCURRING FEES

The present European patent application comprised at the time of filing more than ten claims.

☐ Only part of the claims have been paid within the prescribed time limit. The present European search report has been drawn up for the first ten claims and for those claims for which claims fees have been paid, namely claim(s):

☐ No claims fees have been paid within the prescribed time limit. The present European search report has been drawn up for the first ten claims.

LACK OF UNITY OF INVENTION

The Search Division considers that the present European patent application does not comply with the requirements of unity of invention and relates to several inventions or groups of inventions, namely:

see sheet B

☒ All further search fees have been paid within the fixed time limit. The present European search report has been drawn up for all claims.

☐ As all searchable claims could be searched without effort justifying an additional fee, the Search Division did not invite payment of any additional fee.

☐ Only part of the further search fees have been paid within the fixed time limit. The present European search report has been drawn up for those parts of the European patent application which relate to the inventions in respect of which search fees have been paid, namely claims:

☐ None of the further search fees have been paid within the fixed time limit. The present European search report has been drawn up for those parts of the European patent application which relate to the invention first mentioned in the claims, namely claims:

European Patent Office

LACK OF UNITY OF INVENTION
SHEET B

Application Number
EP 02 25 8114

The Search Division considers that the present European patent application does not comply with the requirements of unity of invention and relates to several inventions or groups of inventions, namely:

1. claims: 1-8 11-13 15-20

A circuit,
with first and second transistors that are coupled to a connection point between a first and a second capacitor of a series of stacked capacitors.

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2. claim: 9 10

A circuit,
with an input reference being a range of voltages.

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3. claims: 14 22 24-28

A circuit,
where the circuit is an active circuit being included in a power supply.

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4. claim: 21

A method,
involving an offset between an upper and a lower reference voltages being substantially zero.

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5. claim: 23

A method,
comprising switching off a first and a second transistor if the voltage at a connection point is between an upper and a lower reference voltage.

ANNEX TO THE EUROPEAN SEARCH REPORT ON EUROPEAN PATENT APPLICATION NO. EP 02 25 8114

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The European Patent Office is in no way liable for these particulars which are merely given for the purpose of information.

26-01-2005

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